GIET POLYTECHNIC, JAGATPUR, CUTTACK

LESSON PLAN

Discipline: ETC	Semester: 3rd	Name Of The Teaching Faculty: Manorama Bhuyan
Subject: Digital Electronics	No. Of Days Per Week Class Allotted: 04 P	Semester From Date: To Date: No. of weeks: 15
Week	Class Day	Theory Topic
1st week	1st	**UNIT1: BASIC OF DIGITAL ELECTRONICS** ➢ 1.1: Number system: binary, octal, decimal, hexadecimal-conversion from one system to another
	2nd	➢ 1.1: Number system: binary, octal, decimal, hexadecimal-conversion from one system to another
	3rd	➢ 1.2: Arithmetic operation(addition, subtraction, multiplication, division),1's & 2's compliment of binary numbers & subtraction using complement method
	4th	➢ 1.2: Arithmetic operation(addition, subtraction, multiplication, division),1's & 2's compliment of binary numbers & subtraction using complement method
2nd week	1st	➢ 1.3: Digital code & its application and distinguish between weighted and non weighted-code,binary code, excess 3 & gray codes
	2nd	➢ 1.3: Digital code & its application and distinguish between weighted and non weighted-code,binary code, excess 3 & gray codes
	3rd	➢ 1.4: Logic gates(AND,OR,NAND,NOR,EX-OR,EX-NOR)-symbol function,expression,truth table & timing diagram
	4th	➢ 1.4: Logic gates(AND,OR,NAND,NOR,EX-OR,EX-NOR)-symbol function,expression,truth table & timing diagram
3rd week	1st	➢ 1.5: Universal gates & realisation
	2nd	➢ 1.6: Boolean Algebra, Boolean expression, Demorgan's theorems
	3rd	➢ 1.7: Represent logic expression : SOP & POS form
	4th	➢ 1.8: K-map (3 & 4 variables) and minimization of logical expression ,Don't care condition
4th week	1st	**UNIT 2: COMBINATIONAL LOGIC CIRCUIT** ➢ 2.1.1: Half adder, full adder
	2nd	➢ 2.1.2: Half subtractor, full subtractor
	3rd	➢ 2.1.3: Serial & parallel binary 4 bit adder
	4th	➢ 2.1.3: Serial & parallel binary 4 bit adder
5th week	1st	➢ 2.2.1: Multiplexer(4:1)
	2nd	➢ 2.2.2: Demultiplexer(1:4)
	3rd	➢ 2.2.3: DECODER
	4th	➢ 2.2.4: ENCODER
6th week	1st	➢ 2.2.5: Digital comparator(3 bit)
	2nd	➢ 2.3:7 segment decoder(definition, gate level of logic circuit)
	3rd	➢ 2.3: 7 segment decoder(truth table & application)
	4th	➢ 2.3: 7 segment decoder(truth table & application
7th week	1st	**UNIT 3: SEQUENTIAL LOGIC CIRCUIT** ➢ 3.1: Principle of flip flop operation, its types
	2nd	➢ 3.1: Principle of flip flop operation, its types
	3rd	➢ 3.2.1: SR flip flop using NAND
	4th	➢ 3.2..2: SR flip flop using NOR Latch(unclocked)
8th week	1st	➢ 3.2..2: SR flip flop using NOR Latch(unclocked)
	2nd	➢ 3.3.1: Clocked SR flip flop (Logic circuit, truth table & application)

	3rd	➢ 3.3.1: Clocked D flip flop (Logic circuit, truth table & application)
8th week	4th	➢ 3.3.1: Clocked JK flip flop (Logic circuit, truth table & application)
9th week	1st	➢ 3.3.1: Clocked T flip flop (Logic circuit, truth table & application)
	2nd	➢ 3.3.1: Clocked JK flip flop (Logic circuit, truth table & application)
	3rd	➢ 3.3.1: Clocked Master slave flip flop (Logic circuit, truth table & application)
	4th	➢ 3.4: Concept of racing and how it can be avoided
10th week	1st	UNIT 4: REGISTERS, MEMORIES & PLD ➢ 4.1.1: Shift register- serial in & serial out, serial in parallel out
	2nd	➢ 4.1.2: Parallel in serial out & parallel in parallel out
	3rd	➢ 4.2: Universal shift registers- applications
	4th	➢ 4.3: Types of counter & application
11th week	1st	➢ 4.4.1: Binary counter , Asynchronous ripple counter(up & down)
	2nd	➢ 4.4.2: Decade counter, synchronous counter, Ring counter
	3rd	➢ 4.5: Concept of memories- RAM, ROM, static RAM, dynamic RAM, PS RAM
	4th	➢ 4.6: Basic concept of PLD & application
12th week	1st	UNIT 5: A/D & D/A CONVERTER ➢ 5.1: Necessity of A/D & D/A converters
	2nd	➢ 5.1: Necessity of A/D & D/A converters
	3rd	➢ 5.2: D/A conversion using weighted resistor methods
	4th	➢ 5.3: D/A conversion using R-2R ladder (Weighted resitors) network
13th week	1st	➢ 5.3: D/A conversion using R-2R ladder (Weighted resitors) network
	2nd	➢ 5.4: A/D conversion using counter method
	3rd	➢ 5.5: Conversion using successive approximate method
	4th	UNIT 6: LOGIC FAMILIES ➢ 6.1: Various logic families & categories according to the IC fabrication process
14th week	1st	➢ 6.1: Various logic families & categories according to the IC fabrication process
	2nd	➢ 6.2.1: Characteristics of Digital ICs- propagation Delay
	3rd	➢ 6.2.2: Characteristics of Digital ICs- fan-out, fan-in, power Dissipation, Noise Margin
	4th	➢ 6.2.3: Characteristics of Digital ICs- power supply requirement & speed with reference to logic families
15th week	1st	➢ 6.3.1: Features, circuit operation & various applications of TTL(NAND)
	2nd	➢ 6.3.1: Features, circuit operation & various applications of CMOS(NAND & NOR)
	3rd	➢ REVISION
	4th	➢ REVISION